CLAIMS

What is claimed is:

1. A method for transferring data between blocks in a design during simulation, comprising:

co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS); and

transferring a first vector of data values received by the first high-level block to the first hardware-implemented block via a single call to a first function provided by an interface that couples the HLMS to the first hardware-implemented block.

2. The method of claim 1, further comprising:

simulating operation of a second high-level block in the design; and

transferring the first vector of data values from the second high-level block to the first high-level block.

3. The method of claim 1, further comprising:

co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements a second high-level block in the design simulated in the HLMS; and

transferring the first vector of data values from the second high-level block to the first high-level block.

4. The method of claim 1, further comprising transferring a second vector of data values received by the interface from the first hardware-implemented block, to the first high-level block in response to a single call to a second function provided by the interface and invoked by the first high-level block.

5. The method of claim 4, further comprising:

simulating operation of a second high-level block in the design in the HLMS; and

transferring the second vector of data values from the first high-level block to the second high-level block.

6. The method of claim 4, further comprising:

co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements a second high-level block in the design simulated in the HLMS; and

transferring the second vector of data values from the first high-level block to the second high-level block.

7. The method of claim 4, wherein the hardware co-simulation platform includes a field programmable gate array (FPGA), and the method further comprises:

determining from the design a required size for a buffer used in transferring a frame of data;

establishing at least one buffer of the required size on the FPGA; and

temporarily storing at least one of a first frame and a second frame in the buffer.

8. The method of claim 7, wherein the determining step comprises for each vector that drives an output port determining an associated size of the vector, wherein the required size of the buffer is equal to the size of the vector.

9. The method of claim 7, wherein the determining step comprises determining the required size as a function of a value of a user-provided configuration parameter.

10. The method of claim 9, wherein the configuration parameter is associated a buffer-size compilation option of

the HLMS.

11. The method of claim 7, wherein one or more input/output ports each has an associated configuration parameter value.

12. The method of claim 7, further comprising:

estimating FPGA resources available for buffers; and

selecting one or more buffer sizes as a function of the estimated available resources.

13. A method for transferring data between blocks in a design during simulation, comprising:

co-simulating a first hardware-implemented block in the design on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS);

accumulating, by the first high-level block in response to a plurality of input scalar values, the plurality of scalar data values in a vector of data; and

transferring the vector of data from the first high-level block to the hardware-implemented block via a single first transfer instruction to an interface that couples the HLMS to the first hardware-implemented block.

14. The method of claim 13, further comprising:

simulating operation of a second high-level block in the design in a high-level modeling system (HLMS); and

transferring the plurality of scalar values from the second high-level block to the first high-level block.

15. The method of claim 13, further comprising:

co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements a second high-level block in the design simulated in the HLMS; and

transferring the plurality of scalar values from the second high-level block to the first high-level block.

16. The method of claim 13, further comprising:

simulating operation of a second high-level block in the design in a high-level modeling system (HLMS); and

outputting a sequence of scalar values from a vector of data received by the first high-level block from the first hardware-implemented block to the second high-level block.

17. The method of claim 13, further comprising:

co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements a second high-level block in the design; and

outputting a sequence of scalar values from a vector of data received by the first high-level block to the second high-level block.

18. The method of claim 13, wherein the hardware co-simulation platform includes a field programmable gate array (FPGA), and the method further comprises:

determining from the design a required size for a buffer used in transferring a frame of data;

establishing at least one buffer of the required size on the FPGA; and

temporarily storing at least one of a first frame and a second frame in the buffer.

19. The method of claim 18, wherein the determining step comprises determining the required size as a function of a value of a user-provided configuration parameter.

20. The method of claim 19, wherein the configuration parameter is associated a buffer-size compilation option of the HLMS.

21. The method of claim 18, wherein one or more input/output ports each has an associated configuration parameter value.

22. The method of claim 18, further comprising:

estimating FPGA resources available for buffers; and

selecting one or more buffer sizes as a function of the estimated available resources.

23. An apparatus for transferring data between blocks in a design during simulation, comprising:

means for co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS); and

means for transferring a first frame of data received by the first high-level block to the first hardware-implemented block via a single call to a first function provided by an interface that couples the HLMS to the first hardware-implemented block.

24. An apparatus for transferring data between blocks in a design during simulation, comprising:

means for co-simulating a first hardware-implemented block in the design on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS);

means for accumulating, by the first second high-level block in response to a plurality of input scalar values, the a plurality of scalar data values in a frame of data; and

means for transferring the frame of data from the first high-level block to the hardware-implemented block via a single first transfer instruction to an interface that couples the HLMS to the first hardware-implemented block.